LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING
(AUTONOMOUS)
Accredited by NAAC & NBA (CSE, IT, ECE, EEE & ME)
Approved by AICTE, New Delhi and Affiliated to JNTUK, Kakinada
L.B.Reddy Nagar, Mylavaram-521230, Krishna Dist, Andhra Pradesh, India
DEPARTMENT OF ELECTRONICS& COMMUNICATION ENGINEERING

Date:05.02.2023

Report on training program of "VLSI Physical Design using Innovus"

Event Type	:	STTP(Short term training Program)
Date / Duration	:	28.01.2023 To 03.02.2023
Resource Person	:	Sudeer, kedarnath
Name of Coordinator(s)	:	G.Venkata Rao and N.Dharmachari
Target Audience	:	VIII- Semester B.Tech Students
Total no of Participants	:	VIII- semester Students-30 Nos.
Objective of the event	:	To reduce the gap between academics and VLSI industry, and to promote the Core VLSI domain in the student community.

Description / Report on Event:

Department of ECE of Lakireddy Bali Reddy College of Engineering (Autonomous), has organized A Six-Days Physical Design Training Program using Innovus In Association with Entuple technologies Pvt. Ltd. under the coordinator-ship of Mr. Venkata Rao G and Mr. Dharma Chari. K. The Program was conducted from 28-01-2023 to 03-02-2023.

ABOUT Training:

With the intention of promoting the core VLSI domain and to reduce the gap between academics and industry into student community we started with training program in Association with Entuple Technologies Pvt. Ltd , Bangalore. In this training students learn much and ready to do their graduation projects in this VLSI domain. We are happy to say few of the students taken this training as a challenge.

OBJECTIVES of STTP:

The objectives of the training program are:

- To reduce the gap between academics and industry
- promoting the core VLSI domain in student community.

Program schedule:

(Day-1)-28th Jan 2023 – By Sudhir, Application Engineer
Session-1:

- Introduction to Semi-Custom IC Design Flow
- Cadence Solutions for Semi-Custom IC Design
- Functional Verification using Incisive
- RTL Synthesis using Genus Synthesis Solution
- Reports and data interpretation for Physical Design

Session-2:

- Introduction for Physical Design flow
- Physical design flow for Block and Chip level
- Introduction to Innovus tools and TCL
- Early PD design preparation
- Physical Design Challenges
- (Floor planning • Congestion • Timing • Runtime)

(Day-2)-29th Jan 2023-By Sudhir, Application Engineer
Session-3:

- Physical Implementation using Innovus that includes
- Floor Planning
- Power Planning
- Placement
- CTS
- Routing

Session-4:

- Timing Analysis
- Power Analysis
- Parasitic Extraction
- Generation of GDSII

(Day-3) -30th Jan 2023-By Navaneetha Krishanav, Sr. AE
Session-5:

- Estimation for Floor plan, Power plan
- Planning for Placement, Types of Placement, Congestion

 Preparations for Clock tree synthesis, Clock skew, Clock tree optimization
 Routing, Types of routing, Crosstalk
 Physical Verification, Timing fixes

Session-6:
 Timing Analysis using Tempus
 Power Analysis using Voltus
 Parasitic Extraction
 Generation of GDSII
Note: By considering 8-Bit Counter/UART/ as an example will demonstrate the entire Semi-Custom IC Design Flow.

(Day-4) – 31th Jan 2023- By Navaneetha Krishanav, Sr. AE
Session-7:
➢ Introduction to IP Design Flow
➢ VLSI Physical Design with Macros
➢ Functional Verification using Conformal LEC Tool
➢ RTL Synthesis using Genus tool

Session-8:
➢ IP Physical Implementation using Innovus that includes
✓ Floor Planning ✓ Power Planning
✓ Placement ✓ CTS ✓ Routing
➢ IP Timing Analysis
➢ IP Power Analysis
➢ Parasitic Extraction
➢ Generation of GDSII

(Day-5) – 1st Feb 2023- By Navaneetha Krishanav, Sr. AE

Session-9:
➢ Introduction to Tempus
➢ Timing Analysis using Tempus

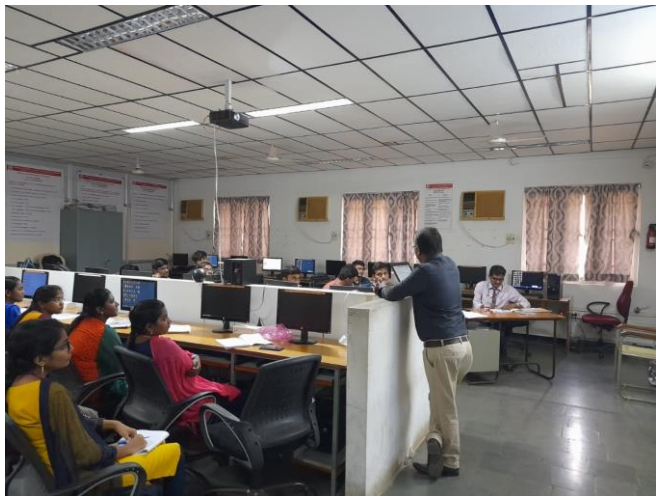
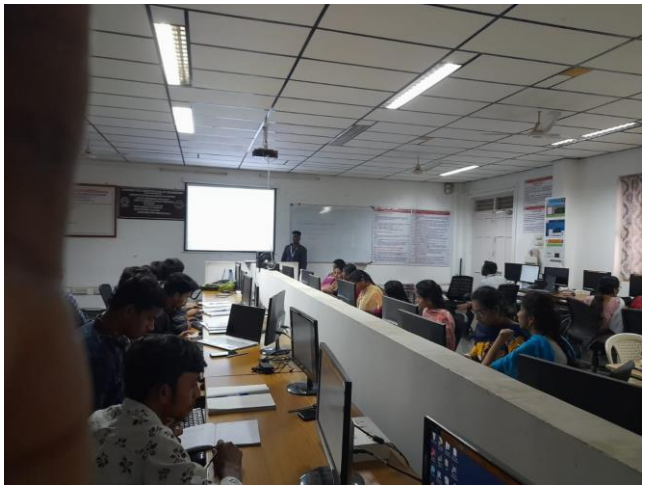
Session-10:
➢ Introduction to Voltus
➢ Power Analysis using Tempus

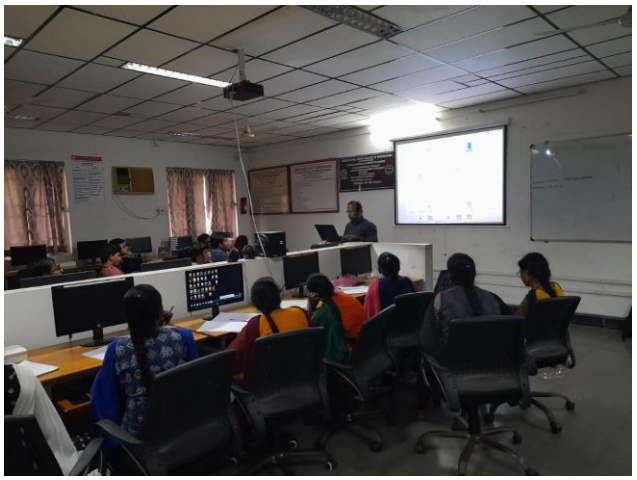
(Day-6) – 3rd Feb 2023
Session-11:
➢ Introduction to SoC Design using Cadence tool
➢ Front-end design flow for MSP430 Processor

➢ Back-end design flow for MSP430 Processor
➢ Generation of GDSII

Session-12:
➢ Discussion on Cadence Innovus Tools integration

Photos:



08.03.2023

Coordinator
(Mr. Venkata Rao G)

(Dr. Y. Amar Babu)

(Mr. Dharma Chari. K)